

**AMENDMENTS TO THE DRAWINGS**

The attached sheet of drawings includes changes to FIG. 4 as described in the “Remarks” section of this amendment. The attached sheet replaces the originally filed sheet containing Figures 4.

Attachment: Replacement sheet containing Figure 4.

### **REMARKS**

The drawings are objected to under 37 CFR § 1.83(a). Figure 4 has been amended to show every feature of the invention specified in the claims, specifically the “channel region ... located below the bottom surface of the gate.” No new matter has been entered. Applicant respectfully submits that all of the figures, including Figure 4, are in proper form.

The specification has been amended to refer to the reference numeral representing the channel region which was added to Figure 4.

Claims 20 and 59 have been amended. Claims 1-37 and 59-65 are pending in this application.

Claim 20 has been allowed but has been amended to correct a clerical error in order to create proper antecedent basis for the claim term “doped surface layer.”

Claims 59-65 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Koizumi et al. (U.S. Patent No. 6,661,459)(“Koizumi”) in view of Yasaka (611-174765 JPO). The rejection is respectfully traversed.

Koizumi relates to a solid state image pickup device. Koizumi at col. 2, lines 60-63. Koizumi’s device includes a pixel having transistors, including transfer and reset transistors. Koizumi at col. 4, lines 16-30; FIG. 3. While Koizumi acknowledges that CCD sensors are known, Koizumi contrasts CCD sensors to Koizumi’s sensor, which is a CMOS sensor (APS) as evidenced by the figures and description. Koizumi at col. 1, lines 12-66; col. 4, line 17 to col. 5, line 66; FIG. 3.

Yasaka relates to a CCD shift register having a structure in which a groove having slant side surfaces is provided in order to increase the width of a transfer channel. Yasaka at Abstract. This in turn increases both the maximum charge amount which can be transferred and the dynamic range. Yasaka at Abstract.

The present invention relates to a pixel cell having a reduced potential barrier in a region where a gate and photodiode are in close proximity to one another. As amended, independent claim 59 recites, *inter alia*, “a gate of a transistor formed in the trench and contained within the lateral boundaries of the trench, the gate having a bottom surface below the surface of the substrate” and “a photo-conversion device formed adjacent to the gate, the photo-conversion device comprising a doped surface layer of a first conductivity type, and a doped region of a second conductivity type underlying the doped surface layer, wherein the doped surface layer is at least partially above a level of a bottom surface of the gate and wherein the second conductivity type layer is at a level below the level of the bottom surface of the gate.”

Both Koizumi and Yasaka fail to teach or suggest these limitations. To overcome the deficiencies of Koizumi, which fails to teach or suggest any gate below the surface of the substrate or within a trench, the Examiner turns to Yasaka. Yasaka, however, shows only capacitor gates, each formed within a groove. Yasaka fails to teach “a photo-conversion device formed adjacent to the gate, the photo-conversion device comprising a doped surface layer of a first conductivity type, and a doped region of a second conductivity type underlying the doped surface layer, wherein the doped surface layer is at least partially above a level of a bottom surface of the gate and wherein the second conductivity type layer is at a level below the level of the bottom surface of the gate.” The N region 6 (second conductivity type layer) of Yasaka is not at a level below the level of the bottom surface of the transfer electrodes 2/3. Thus, the cited combination of Koizumi and Yasaka do not teach or suggest the limitations of claim 59.

Additionally, one of ordinary skill in the art would not have been motivated to combine the teachings of Koizumi and Yasaka in the manner suggested by the Examiner. The Examiner states that one of ordinary skill in the art would have been motivated to combine Koizumi and Yasaka to “substantially increase the width of the transfer channel in order to increase the maximum charge transferred, and obtain a broader dynamic range.” Office Action dated June 27, 2005. Yasaka relates to CCD sensors and the groove in Yasaka (see FIG. 1) acts to hold the CCD shift register. In contrast, Koizumi teaches a CMOS sensor, or active pixel sensor (APS), having a transfer MOS transistor above the region between the photodiode and floating diffusion region. When the transfer transistor is in an off state, charge can be

accumulated in the photodiode. When a voltage is applied to Koizumi's transfer transistor gate, charge is transferred to the floating diffusion region. Koizumi at col. 5, lines 17-66. Thus, the transfer transistor is not operated to form a storage region, and is configured to operate differently than the transfer electrodes of Yasaka.

Yasaka teaches that the dynamic range is increased by widening the transfer channel because the larger gate can store more charge. The motivation to "increase the width of the transfer channel in order to ... obtain a broader dynamic range" found in Yasaka would not apply to the transfer transistor of Koizumi since it isn't a storage device.

The teachings of Yasaka, therefore, are not interchangeable with those of Koizumi as suggested by the Examiner. There is nothing in the references to suggest combining these teachings. Thus, those of ordinary skill in the art would not have been motivated to combine the teachings of Koizumi and Yasaka to achieve the claimed invention.

Claims 60-65 are dependent on claim 59 and should be allowed for the reasons stated above as well as other reasons.

In view of the above amendment, applicants believe the pending application is in condition for allowance.

Dated: September 27, 2005

Respectfully submitted,

By 

Thomas J. D'Amico

Registration No.: 28,371

Jennifer M. McCue

Registration No.: 55,440

DICKSTEIN SHAPIRO MORIN & OSHINSKY  
LLP

2101 L Street NW

Washington, DC 20037-1526

(202) 785-9700

Attorneys for Applicants

Attachments